What is claimed is:

1. A semiconductor device comprising:

an instruction memory storing an instruction program consisting of instruction codes, said instruction program being stored as data associated with an address;

an instruction fetch block for fetching said instruction program data;

a decode block for decoding said instruction codes; and

an execution block for executing a decoded instruction according to a control signal associated with said decoded instruction;

wherein

said address is provided from said instruction fetch block to said instruction memory, said instruction program data at said address is inputted from said instruction memory to said instruction fetch block, the instruction code associated with said instruction program data is inputted from said instruction fetch block to said decode block, the control signal associated with the instruction decoded from said instruction code is inputted from said decode block into said execution block, a conditional-branch-taken signal indicating a status of a conditional branch is outputted from said execution block, said status depending on a result of the execution of the instruction according to the control signal, and the execution of the conditional branch is controlled according to the instruction program in said instruction memory, said execution depending on the conditional-branch-taken signal, and

said semiconductor device comprising a controller for selecting one of a branch target address to be used if the

conditional branch is taken and an address to be used if the conditional branch is not taken on the basis of a condition of said conditional-branch-taken signal and providing said address to said instruction memory during a fetch performed by said instruction fetch block.

2. The semiconductor device according to claim 1, wherein said branch target address is generated from displacement information included in said instruction program data.

3. The semiconductor device according to claim 2, further comprising a determiner for determining a conditional branch instruction on the basis of the instruction code provided from said instruction fetch block, wherein the execution of the conditional branch instruction is detected on the basis of a result of the determination and, only when said conditional branch instruction is executed, the address selection based on said conditional-branch-taken signal is made.

4. The semiconductor device according to claim 2, wherein said instruction memory consists of memory cells arranged in two-dimensional arrays for two-dimensionally addressing the addresses in said instruction memory and said conditional-branch-taken signal is provided as an address selection signal to the output of one of two address decoders, each of which being associated with each of said two-dimensional arrays, said one of the two address decoder being determined after the other.

5. The semiconductor device according to claim 2, wherein said instruction memory consists of memory cells arranged in two-dimensional arrays for two-dimensionally addressing the addresses in said instruction memory and said conditional-branch-taken signal is provided as an address selection signal to the input of one of the two address decoders, each of which being associated with each of said two-dimensional arrays, said one of the two-address decoder being determined after the other.

6. The semiconductor device according to claim 3, wherein said instruction memory consists of memory cells arranged in two-dimensional arrays for two-dimensionally addressing the addresses in said instruction memory and said conditional-branch-taken signal is provided as an address selection signal to the output of one of the two address decoders, each of which being associated with each of said two-dimensional arrays, said one of the two-address decoders being determined after the other.

7. The semiconductor device according to claim 3, wherein said instruction memory consists of memory cells arranged in two-dimensional arrays for two-dimensionally addressing the addresses in the instruction memory and said conditional-branch-taken signal is provided as an address selection signal to the input of one of the two address decoders, each of which being associated with each of said two-dimensional arrays, said one of the two address decoders being determined after the other.

8. The semiconductor device according to claim 3, wherein said instruction memory consists of memory cells arranged in two-dimensional arrays for two-dimensionally addressing the addresses in said instruction memory, and the address of a conditional branch instruction and the address of a branch target instruction are mapped by a linker so that an address input into one of the address decoders associated with said two-dimensional arrays remains the same, said one of the address decoders being determined before the other, and an address input into the other address decode changes.